In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1. (Cancelled)

2. (Currently Amended) The CPU of claim 3 ~~1~~ wherein the mapping logic function distributes entries within the TLB throughout the TLB.

3. (Currently Amended) A central processing unit (CPU) comprising:

a translation lookaside buffering; and

a mapping logic function to predict a set index value for the TLB prior to the generation of an effective address, ~~The CPU of claim 1 wherein~~ the mapping logic having ~~comprises~~ a N-bit add modulo 2^N function of base-register bits and offset bits of a virtual address, where N is smaller than the number of bits in a virtual address.

4. (Currently Amended) A central processing unit (CPU) comprising:

a translation lookaside buffering; and

a mapping logic function to predict a set index value for the TLB prior to the generation of an effective address, ~~The CPU of claim 1 wherein~~ the mapping logic having ~~comprises~~ an Exclusive-or of some number of base-register bits and some number of offset bits of a virtual address.

5. (Currently Amended) The CPU of claim 4 ~~1~~ further comprising a register interface having one or more registers to control the TLB.

6. (Original) The CPU of claim 5 wherein the one or more registers within the register interface chooses an entry within the TLB to be accessed.

7. (Currently Amended) A central processing unit (CPU) comprising:

a translation lookaside buffering; and

a mapping logic function to predict a set index value for the TLB prior to the generation of an effective address, ~~The CPU of claim 1~~ wherein the predicted set index may differ from the effective address without requiring recovery actions if the predicted set index and the effective address differ.

8. (Currently Amended) The CPU of claim 7 ~~1~~ wherein mapping logic function includes a first set of bits from instruction and a second set of bits from base and offset addresses.

9. (Currently Amended) The CPU of claim 7 ~~1~~ wherein the effective address being mapped is the address of an instruction that is being fetched for execution.

10. (Currently Amended) The CPU of claim 7 ~~1~~ wherein the effective address being mapped is the address of data being read or written by the processor.

11. (Currently Amended) A central processing unit (CPU) comprising:

a translation lookaside buffering; and

a mapping logic function to predict a set index value for the TLB prior to the generation of an effective address, ~~The CPU of claim 1 wherein~~ the mapping logic function includes control signals received from the processor and bits received from the generation of the effective address.

12. (Original) The CPU of claim 11 wherein the mapping logic combines the signals and the bits using a hash to predict a set to look up the translation for the predicted address.

13. (Currently Amended) A method comprising:

looking up a register at a register interface; and

predicting a set index value for a translation lookaside buffer (TLB) at a mapping logic function having an Exclusive-or of some number of base-register bits and some number of offset bits of a virtual address prior to the generation of an effective address.

14. (Original) The method of claim 13 further comprising performing a lookup of the TLB using the predicted set index.

15. (Original) The method of claim 13 further comprising calculating an effective address.

16. (Original) The method of claim 13 wherein the predicted set index differs from the effective address.

17. (Cancelled)

18. (Currently Amended) The computer system of claim 19 ~~17~~ wherein the mapping logic function distributes entries within the TLB throughout the TLB.

19. (Currently Amended) A computer system comprising central processing unit (CPU) having a mapping logic function to predict a set index value for a translation lookaside buffer (TLB) prior to the generation of an effective address, ~~The computer system of claim 17 wherein~~ the mapping logic function having ~~comprises~~ a N-bit add modulo 2^N function of base-register bits and offset bits of a virtual address, where N is smaller than the number of bits in a virtual address.

20. (Currently Amended) The computer system of claim 19 ~~17~~ wherein the mapping logic function comprises an Exclusive-or of some number of base-register bits and some number of offset bits of a virtual address.

21. (Currently Amended) The computer system of claim 19 ~~17~~ further comprising a register interface having one or more registers to control the TLB.

22. (Original) The computer system of claim 21 wherein the one or more registers within the register interface chooses an entry within the TLB to be accessed.

23. (Currently Amended) The computer system of claim 19 ~~17~~ wherein the mapping logic function includes control signals received from the processor and bits received from the generation of the effective address.

24. (Original) The computer system of claim 23 wherein the mapping logic combines the signals and the bits using a hash to predict a set to look up the translation for the predicted address.

25. (Cancelled)

26. (Currently Amended) The computer system of claim 27 ~~25~~ wherein the mapping logic function distributes entries within the TLB throughout the TLB.

27. (Currently Amended) A computer system comprising: ~~The computer system of claim 25 wherein~~

central processing unit (CPU) having a mapping logic function to predict a set index value for a translation lookaside buffer (TLB) prior to the generation of an effective address, the mapping logic having ~~comprises~~ a N-bit add modulo 2^N function of base-register bits and offset bits of a virtual address, where N is smaller than the number of bits in a virtual address;

a chipset coupled to the CPU and

a main memory coupled to the chipset.